CLAIMS

1. A functional block for integrated circuit, characterized by comprising a test data output circuit for outputting test data responsive to a control signal indicating a test data transmission state.

2. The functional block for integrated circuit of Claim 1, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output, and

outputs the test data such that an adjacent pair of the output signal lines have mutually different values.

3. The functional block for integrated circuit of Claim 1, characterized in that the test data output circuit outputs the test data changing from one value into the other.

4. The functional block for integrated circuit of Claim 1, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output, and

outputs the test data such that an adjacent pair of the output signal lines have mutually different values, and that each of the output signal lines outputs the test data alternately changing from one value into the other and vice versa.

5. The functional block for integrated circuit of Claim 1, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output,

divides the output signal lines into a number 2^n of groups, where n is an integer equal to or larger than one, and

outputs the test data such that the respective groups divided have mutually different values, which change from one value into the other.

6. The functional block for integrated circuit of Claim 1, characterized in that the test data output circuit includes:

an original data generating section for generating and outputting first and second original data, the first original data being composed of zeros and ones alternately arranged, the second original data being obtained by inverting the first original data; and

a selector circuit for receiving the first and second original data and selecting either the first or second original data in response to a selection signal externally supplied, thereby outputting the test data.

7. The functional block for integrated circuit of Claim 6, characterized in that the test data output circuit includes a plurality of the selector circuits, and

further includes a shift register for receiving the selection signal and outputting the input selection signal to each said selector circuit.

8. The functional block for integrated circuit of Claim 1, characterized in that the test data output circuit includes:

an original data generating section for generating and outputting original data composed of zeros and ones alternately arranged; and

a plurality of inverter circuits, each receiving the original data, and

that control signals with mutually inverted values are input to the inverter circuits, which output the test data with mutually inverted values.

9. The functional block for integrated circuit of Claim 8, characterized in that the test data output circuit further comprises a shift register for receiving the control signal and outputting the input control signal to each said inverter circuit.

10. The functional block for integrated circuit of Claim 1, characterized in that the test data output circuit includes:

a plurality of test data generating sections for generating mutually different test data; and

a test data selecting section for selecting one of the test data generating sections responsive to the control signal.

11. The functional block for integrated circuit of Claim 1, characterized by further comprising a decision result output circuit for receiving the test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision.

12. The functional block for integrated circuit of Claim 1, characterized by further comprising a testing standby circuit for blocking the output of an output signal responsive to a control signal indicating a testing standby state.

13. The functional block for integrated circuit of Claim 12, characterized in that the test data output circuit includes an inverted data generating section for inverting a value of the test data responsive to the control signal indicating the testing standby state.

14. The functional block for integrated circuit of Claim

1, characterized by further comprising:

a decision result output circuit for receiving the test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision; and

a testing standby circuit for blocking the output of an output signal responsive to a control signal indicating a testing standby state.

15. The functional block for integrated circuit of Claim 14, characterized in that the test data output circuit includes an inverted data generating section for inverting a value of the test data responsive to the control signal indicating the test data reception state.

16. A functional block for integrated circuit, characterized by comprising a decision result output circuit for receiving test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision.

17. The functional block for integrated circuit of Claim 16, characterized in that the decision result output circuit

includes a plurality of expected value comparing sections, each comparing the test data to an expected value of the test data.

18. The functional block for integrated circuit of Claim 16, characterized in that on deciding that the test data is erroneous, the decision result output circuit outputs the decision result.

19. The functional block for integrated circuit of Claim 16, characterized in that the decision result output circuit includes holding means for holding the decision result thereon.

20. The functional block for integrated circuit of Claim 19, characterized in that the holding means is a shift register.

21. The functional block for integrated circuit of Claim 16, characterized by further comprising a testing standby circuit for blocking the output of an output signal responsive to a control signal indicating a testing standby state.

22. A functional block for integrated circuit characterized by comprising a testing standby circuit for blocking the

output of an output signal responsive to a control signal indicating a testing standby state.

23. A semiconductor integrated circuit characterized by comprising:

a first functional block including a test data output circuit for outputting test data responsive to a first control signal indicating a test data transmission state;

a second functional block for integrated circuit, including a decision result output circuit for receiving the test data responsive to a second control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision;

a test control output section for outputting the first and second control signals to the first and second functional blocks for integrated circuit, respectively; and

a test result output circuit for receiving a decision result signal from the decision result output circuit and outputting the received decision result signal as a test result signal.

24. The semiconductor integrated circuit of Claim 23, characterized by further comprising:

an output signal line including a plurality of signal

paths interconnecting the first and second functional blocks for integrated circuit together; and

a switching circuit, which is connected to the output signal line, for switching the signal paths by selecting one of the signal paths, and

characterized in that the test data output circuit outputs a path control signal for controlling the switching circuit.

25. The semiconductor integrated circuit of Claim 23, characterized in that the test result output circuit outputs the test result on receiving the decision result.

26. The semiconductor integrated circuit of Claim 23, characterized in that the test result output circuit includes holding means for holding the decision result thereon.

27. The semiconductor integrated circuit of Claim 23, characterized by further comprising a third functional block for integrated circuit, including a testing standby circuit for blocking the output of an output signal responsive to a third control signal indicating a testing standby state, and

characterized in that the test control output section outputs the third control signal to the third functional block for integrated circuit.

28. The semiconductor integrated circuit of Claim 27, characterized by further comprising:

an output signal line including a plurality of signal paths interconnecting one of the first, second and third functional blocks for integrated circuit to the other ones; and

a switching circuit, which is connected to the output signal line, for switching the signal paths by selecting one of the signal paths, and

characterized in that the test data output circuit outputs a path control signal for controlling the switching circuit.

29. The semiconductor integrated circuit of Claim 23, characterized in that a plurality of the second functional blocks for integrated circuit are provided, and

that each said second functional block for integrated circuit includes a shift register for holding the decision result thereon, and

that the shift registers are connected together to form a single composite shift register.

30. A method for testing a semiconductor integrated circuit, the semiconductor integrated circuit comprising: a first functional block including a test data output circuit for

outputting test data responsive to a first control signal indicating a test data transmission state; a second functional block for integrated circuit, including a decision result output circuit for receiving the test data responsive to a second control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision; a third functional block for integrated circuit, including a testing standby circuit for blocking the output of an output signal responsive to a third control signal indicating a testing standby state; a test control output section for outputting the first, second and third control signals to the first, second and third functional blocks for integrated circuit, respectively; and a test result output circuit for receiving a decision result signal from the decision result output circuit and outputting the received decision result signal as a test result signal, the method characterized by comprising:

a test data transmitting step for making the test control output section output the first control signal to make the test data output circuit of the first functional block for integrated circuit output the test data;

a test data receiving step for making the test control output section output the second control signal to make the decision result output circuit of the second functional block for integrated circuit, which is connected to the first func-

tional block for integrated circuit, receive the test data;

a testing standby step for making the test control output section output the third control signal to make the testing standby circuit of the third functional block for integrated circuit, which is connected to the first functional block for integrated circuit, block the output; and

a test result reading step for reading the test result from the test result output circuit.

31. The method for testing a semiconductor integrated circuit of Claim 30, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output, and

that the test data transmitting step includes:

an initial signal line dividing step for dividing the output signal lines into two groups and outputting the test data through the output signal lines such that the respective groups divided have mutually different values, which change from one value into the other;

a signal line dividing step for dividing each said group into two groups and outputting the test data through the output signal lines such that the respective groups divided have mutually different values, which change from one value into the other; and

a testing step for repeatedly performing the signal line

dividing step until the output signal line belonging to each said group is no longer divisible.

32. A method for designing a semiconductor integrated circuit using a plurality of functional blocks for integrated circuit, each said functional block for integrated circuit performing a predetermined function of a logic or memory circuit, the method characterized by comprising:

a functional block designing step for introducing, into each of the functional blocks for integrated circuit, at least one of: a test data output circuit for outputting test data responsive to a control signal indicating a test data transmission state; a decision result output circuit for receiving the test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision; and a testing standby circuit for blocking the output of an output signal responsive to a control signal indicating a testing standby state;

a functional block library forming step for forming a library of functional blocks by registering the functional blocks for integrated circuit, which have been made in the functional block designing step, at the library; and

a functional block selecting step for selecting such a functional block for integrated circuit as enabling a desired

semiconductor integrated circuit from the functional blocks for integrated circuit that are included in the library of functional blocks.